

SHARP

LH168B/LH168G

324 Outputs 64 Gradations
TFT-LCD Source Driver

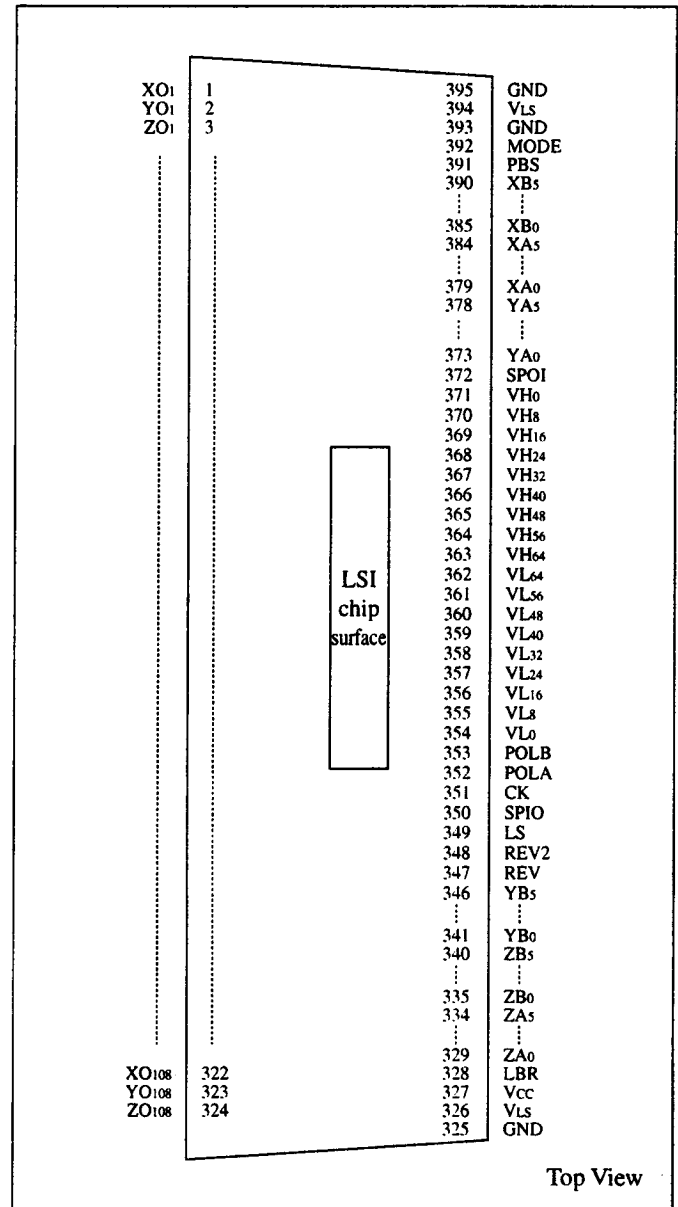
■ Description

The LH168B/LH168G are a source driver with 324 LCD drive outputs, and are used for the TFT LCD unit which can simultaneously display 262 144 colors in 64 gradations.

■ Features

1. The LH168B/LH168G are a driver which incorporates a 6-bit digital input DAC.
2. The LH168B/LH168G are a Dot-Inversion driver that the LCD drive pin inverted gradational voltage at the next LCD drive pins.
3. The number of LCD drive output is 324 outputs and they can change to 321 outputs, 312 outputs and 309 outputs.
4. The circuit of data input have two port inputs at the number of LCD drive outputs is 324 outputs and 312 outputs. They can sample & hold display data of two pixels at the sametime. And the circuit of data input have one port inputs at the number of LCD drive outputs is 321 outputs or 309 outputs.
5. The basic voltage input of 18 gradations can display 262 144 colors in 64 gradations. This basic voltage input corresponds to γ correction and the intermediate basic voltage input can be abbreviated.
6. Shift clock frequency is 55 MHz (MAX.).
7. The LH168B/LH168G have the function of cascade connection.
8. It is possible to switch the output directivity of LCD drive output.
($XO_1, YO_1, ZO_1 \rightarrow XO_{108}, YO_{108}, ZO_{108}$ and $ZO_{108}, YO_{108}, XO_{108} \rightarrow ZO_1, YO_1, XO_1$)
9. Supply voltage V_{CC} for the digital system : 2.7 to 3.6 V
10. Supply voltage V_{LS} for the analog system : 8.0 to 13.0 V
11. Package SST

■ Pin Connections

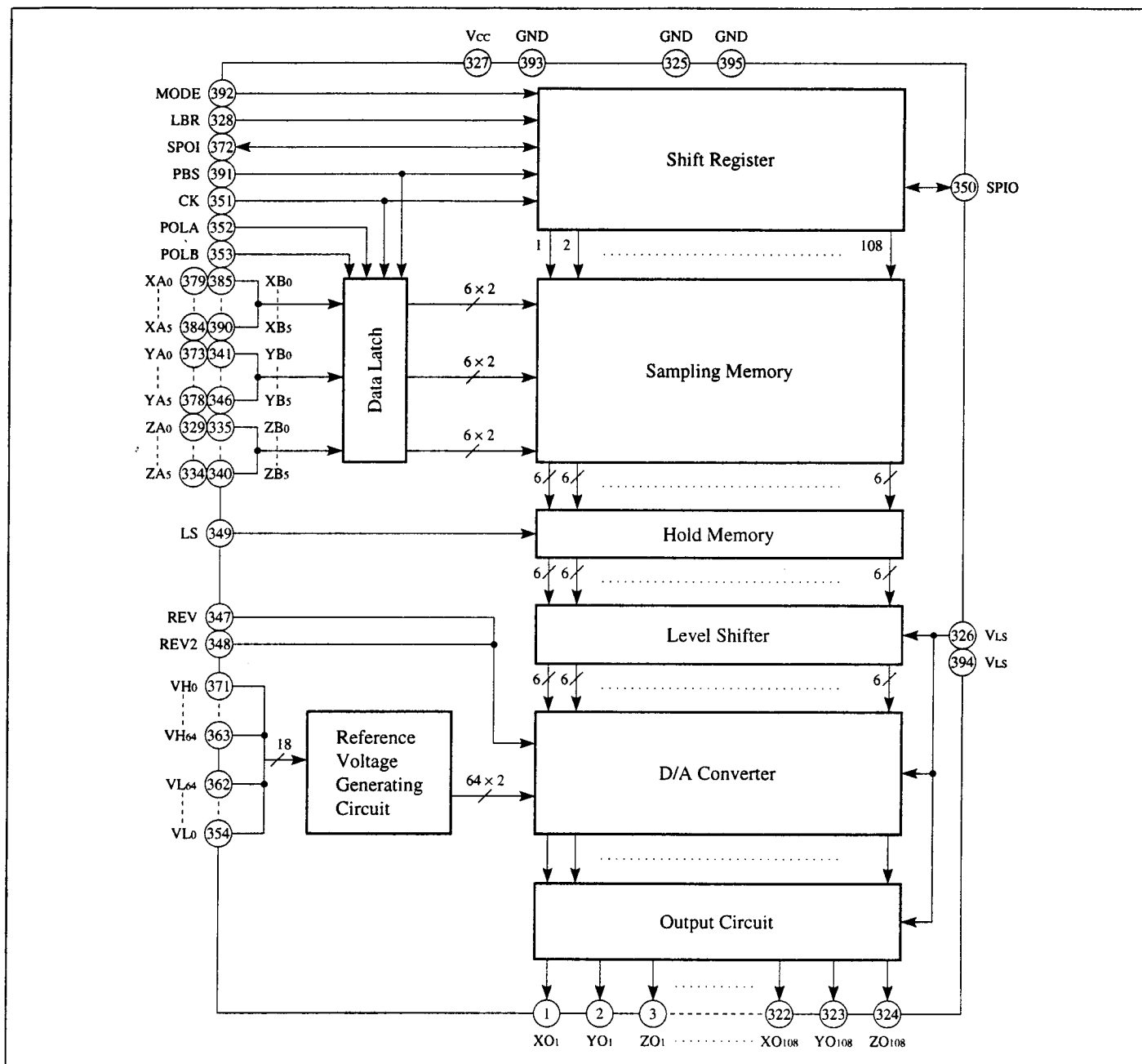


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■ Pin Description

No.	Symbol	I/O	Pin name
1-324	XO ₁ -ZO ₁₀₈	O	LCD drive output pins
325	GND	—	GND
326	V _{LS}	—	Power supply pin for analog circuit
327	V _{CC}	—	Power supply pin for digital circuit
328	LBR	I	Shift direction switching input pin
329-334	ZA ₀ -ZA ₅	I	Data input pins
335-340	ZB ₀ -ZB ₅	I	Data input pins
341-346	YB ₀ -YB ₅	I	Data input pins
347	REV	I	LCD drive output polarity exchange input pin
348	REV ₂	I	LCD drive output polarity exchange input pin
349	LS	I	Latch input pin
350	SPIO	I/O	Start pulse input/cascade output pin
351	CK	I	Shift clock input pin
352	POLA	I	Input data polarity exchange input pin
353	POLB	I	Input data polarity exchange input pin
354-362	VL ₀ -VL ₆₄	I	Reference voltage input pins
363-371	VH ₆₄ -VH ₀	I	Reference voltage input pins
372	SPOI	I/O	Start pulse input/cascade output pin
373-378	YA ₀ -YA ₅	I	Data input pins
379-384	XA ₀ -XA ₅	I	Data input pins
385-390	XB ₀ -XB ₅	I	Data input pins
391	PBS	I	2 ports/1 port switching input pin
392	MODE	I	Number of LCD drive output switching input pin
393	GND	—	GND
394	V _{LS}	—	Power supply pin for analog circuit
395	GND	—	GND

■ Block Diagram



■ Block Function

Block name	Block function
Shift register	Used as a bi-directional shift register, which performs the shifting operation by CK and selects bits for data sampling.
Data latch	Used to temporarily latch the input data, which is sent to the sampling memory.
Sampling memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for temporary latch processing of data in the sampling memory by LS input.
Level shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and send the shifted data to D/A converter.
Reference voltage generating circuit	Used to generate a 64 × 2-level voltage corrected of gamma by the resistance split circuit.
D/A converter	Used to generate analog signal according to the displayed data and send the signal to the output circuit.
Output circuit	Used as a voltage follower configured with an operational amplifier and an output buffer, which outputs analog signals of 64 × 2 gradations to LCD drive output pin.

■ Description of Functions and Operations

(1) Pin function

Symbol	I/O	Function
V _{CC}	—	Used as power supply pin for digital circuit (Use in the range of 2.7 to 3.6 V.)
V _{LS}	—	Used as power supply pin for analog circuit (Use in the range of 8 to 13V.)
GND	—	Used as GND pin, which must be connected to 0 V.
SPIO SPOI	I/O	Used as input pin of start pulse and is also used as output pin for cascade connection. When "High" is input into start pulse input pin, data sampling is started. On completion of sampling, "High" pulse is output to output pin for cascade connection. Pin functions are switched by LBR. For relations of switching, refer to "(2) Operation of function".
LBR	I	Used as input pin for switch shift register directivity. For relations of switching, refer to "(2) Operation of function".
LS	I	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at rising edge and output from LCD drive output pin.
CK	I	Used as shift clock input pin. Data is latched into sampling memory from data input pin at rising edge.
VH ₀ -VH ₆₄ VL ₀ -VL ₆₄	I	Used as basic voltage input pin. Hold the basic potential before outputting gradation voltage. For relation between displayed data and output voltage value, refer to "(4) Output voltage value". For internal gamma correction, refer to "(5) Gamma correction value". Observe the following relation for input potential. V _{LS} > VH ₀ > VH ₈ > ... > VH ₆₄ > VL ₆₄ > VL ₅₆ > ... > VL ₀ > GND.
XA ₀ -XA ₅ YA ₀ -YA ₅ ZA ₀ -ZA ₅ XB ₀ -XB ₅ YB ₀ -YB ₅ ZB ₀ -ZB ₅	I	Used as data input pin of R, G, and B colors. Takes in 6-bits data from data pin at rising edge of CK. When PBS is "Low", taken in 2-pixels data at the sametime from XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ and XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ . When PBS is "High", taken in 1-pixel data from XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ . Fix XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ to "Low" or "High". For relation between input data and output, refer to "(4) Output voltage value". Correlate data to be entered into X, Y, and Z according to picture element arrays of the panel used.
MODE	I	Used as input pin for switch number of LCD drive output, which sets up operation mode with PBS pin. When "Low" is entered, it is 324 outputs/2 ports input mode becomes enable at PBS pin is "Low" or 321 outputs/1 port input mode becomes enable at PBS pin is "High". When "High" is entered, it is 312 outputs/2 ports input mode becomes enable at PBS pin is "Low" or 309 outputs/1 port becomes enable at PBS pin is "High". For relations of switching number or LCD drive output, refer to "(3) Operation mode and output polarity".
PBS	I	Used as 2 ports/1 port exchange input pin to take in data. When "Low" is entered, it is 2 ports input mode becomes enable and takes in 2-pixels data at the sametime. When "High" is entered, it is 1 port input mode becomes enable.
XO ₁ -XO ₁₀₈ YO ₁ -YO ₁₀₈ ZO ₁ -ZO ₁₀₈	O	Used as LCD drive output pin, which outputs the voltage corresponding to the input of data input pin. In the case of 321 outputs mode, 3 outputs (XO ₅₄ -ZO ₅₄) is invalid. In the case of 312 outputs mode, 12 outputs (XO ₅₅ -XO ₅₈ , YO ₅₅ -YO ₅₈ , ZO ₅₅ -ZO ₅₈) is invalid. In the case of 309 outputs mode, 15 outputs (XO ₅₄ -XO ₅₈ , YO ₅₄ -YO ₅₈ , ZO ₅₄ -ZO ₅₈) is invalid. Invalid output pins must be open. Data of XO ₁ -XO ₁₀₈ correspond to XA ₀ -XA ₅ , XB ₀ -XB ₅ . Data of YO ₁ -YO ₁₀₈ correspond to YA ₀ -YA ₅ , YB ₀ -YB ₅ , and data of ZO ₁ -ZO ₁₀₈ correspond to ZA ₀ -ZA ₅ , ZB ₀ -ZB ₅ . For relation of switching and input data, refer to "(2) Operation of function" and "(4) Output voltage value".

Symbol	I/O	Function
POLA POLB	I	Used as input pin for input data polarity exchange, POLA corresponds to XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , POLB corresponds to XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ . When "Low" is entered, displayed data is normal mode becomes enable. When "High" is entered, input data is polarity exchange mode becomes enable. For relation between input data and output, refer to "(4) Output voltage value". This pins are pull-down at the inside.
REV REV ₂	I	Used as polarity exchange pin of LCD drive output. Takes in data at the term that LS is "High", decides output polarity of LCD drive output pin. Function of REV is the same as function of REV ₂ . Input polarity exchange signal to REV pin and REV ₂ is used to fix to "Low" or be open in generally. In the case of 321 outputs/309 outputs mode, it is possible to exchange output polarity between next driver by REV ₂ is fixed to "Low" or "High" according to position on panel. For switching relation, refer to "(3) Operational mode and output polarity". REV ₂ pin is pull-down at the inside.

(2) Operation of function

The following describes the relation between data input pin and output direction.

○PBS = "Low"

Data input pin	XA ₀ -XA ₅	YA ₀ -YA ₅	ZA ₀ -ZA ₅	XB ₀ -XB ₅	YB ₀ -YB ₅	ZB ₀ -ZB ₅	XB ₀ -XB ₅	YB ₀ -YB ₅	ZB ₀ -ZB ₅
Output direction	XO ₁	YO ₁	ZO ₁	XO ₂	YO ₂	ZO ₂	XO ₁₀₈	YO ₁₀₈	ZO ₁₀₈

○PBS = "High"

Data input pin	XA ₀ -XA ₅	YA ₀ -YA ₅	ZA ₀ -ZA ₅	XA ₀ -XA ₅	YA ₀ -YA ₅	ZA ₀ -ZA ₅	XA ₀ -XA ₅	YA ₀ -YA ₅	ZA ₀ -ZA ₅
Output direction	XO ₁	YO ₁	ZO ₁	XO ₂	YO ₂	ZO ₂	XO ₁₀₈	YO ₁₀₈	ZO ₁₀₈

The following describes the relation between LBR pin, SP pin and output direction.

Pin	RIGHT SHIFT (Shift register directivity)	LEFT SHIFT (Shift register directivity)
LBR	"High"	"Low"
SPOI	Input	Output
SPIO	Output	Input
Output direction	XO ₁ , YO ₁ , ZO ₁ (first clock) → XO ₁₀₈ , YO ₁₀₈ , ZO ₁₀₈ (last clock)	ZO ₁₀₈ , YO ₁₀₈ , XO ₁₀₈ (first clock) → ZO ₁ , YO ₁ , XO ₁ (last clock)

Note. Color data corresponding to X, Y and Z vary depending on RIGHT SHIFT/LEFT SHIFT.

(3) Operational mode and output polarity

The following describes the relation between operational mode, REV pin, REV₂ pin and output polarity of LCD drive output pin.

MODE	In the case of REV = "Low", REV ₂ = "Low" or REV = "High", REV ₂ = "High"				In the case of REV = "High", REV ₂ = "Low" or REV = "Low", REV ₂ = "High"			
	"Low"	"Low"	"High"	"High"	"Low"	"Low"	"High"	"High"
PBS Operation	"Low"	"High"	"Low"	"High"	"Low"	"High"	"Low"	"High"
	324 out	321 out	312 out	309 out	324 out	321 out	312 out	309 out
XO ₁	-	-	-	-	+	+	+	+
YO ₁	+	+	+	+	-	-	-	-
ZO ₁	-	-	-	-	+	+	+	+
XO ₂	+	+	+	+	-	-	-	-
YO ₂	-	-	-	-	+	+	+	+
ZO ₂	+	+	+	+	-	-	-	-
.....								
XO ₅₃	-	-	-	-	+	+	+	+
YO ₅₃	+	+	+	+	-	-	-	-
ZO ₅₃	-	-	-	-	+	+	+	+
XO ₅₄	+	NA	+	NA	-	NA	-	NA
YO ₅₄	-	NA	-	NA	+	NA	+	NA
ZO ₅₄	+	NA	+	NA	-	NA	-	NA
XO ₅₅	-	+	NA	NA	+	-	NA	NA
YO ₅₅	+	-	NA	NA	-	+	NA	NA
ZO ₅₅	-	+	NA	NA	+	-	NA	NA
XO ₅₆	+	-	NA	NA	-	+	NA	NA
YO ₅₆	-	+	NA	NA	+	-	NA	NA
ZO ₅₆	+	-	NA	NA	-	+	NA	NA
XO ₅₇	-	+	NA	NA	+	-	NA	NA
YO ₅₇	+	-	NA	NA	-	+	NA	NA
ZO ₅₇	-	+	NA	NA	+	-	NA	NA
XO ₅₈	+	-	NA	NA	-	+	NA	NA
YO ₅₈	-	+	NA	NA	+	-	NA	NA
ZO ₅₈	+	-	NA	NA	-	+	NA	NA
XO ₅₉	-	+	-	+	+	-	+	-
YO ₅₉	+	-	+	-	-	+	-	+
ZO ₅₉	-	+	-	+	+	-	+	-
.....								
XO ₁₀₇	-	+	-	+	+	-	+	-
YO ₁₀₇	+	-	+	-	-	+	-	+
ZO ₁₀₇	-	+	-	+	+	-	+	-
XO ₁₀₈	+	-	+	-	-	+	-	+
YO ₁₀₈	-	+	-	+	+	-	+	-
ZO ₁₀₈	+	-	+	-	-	+	-	+

Note. + : The gradation voltage corresponding to the basic voltage VH₀-VH₆₄ is output.
 - : The gradation voltage corresponding to the basic voltage VL₀-VL₆₄ is output.
 NA : Non active. Must be open.

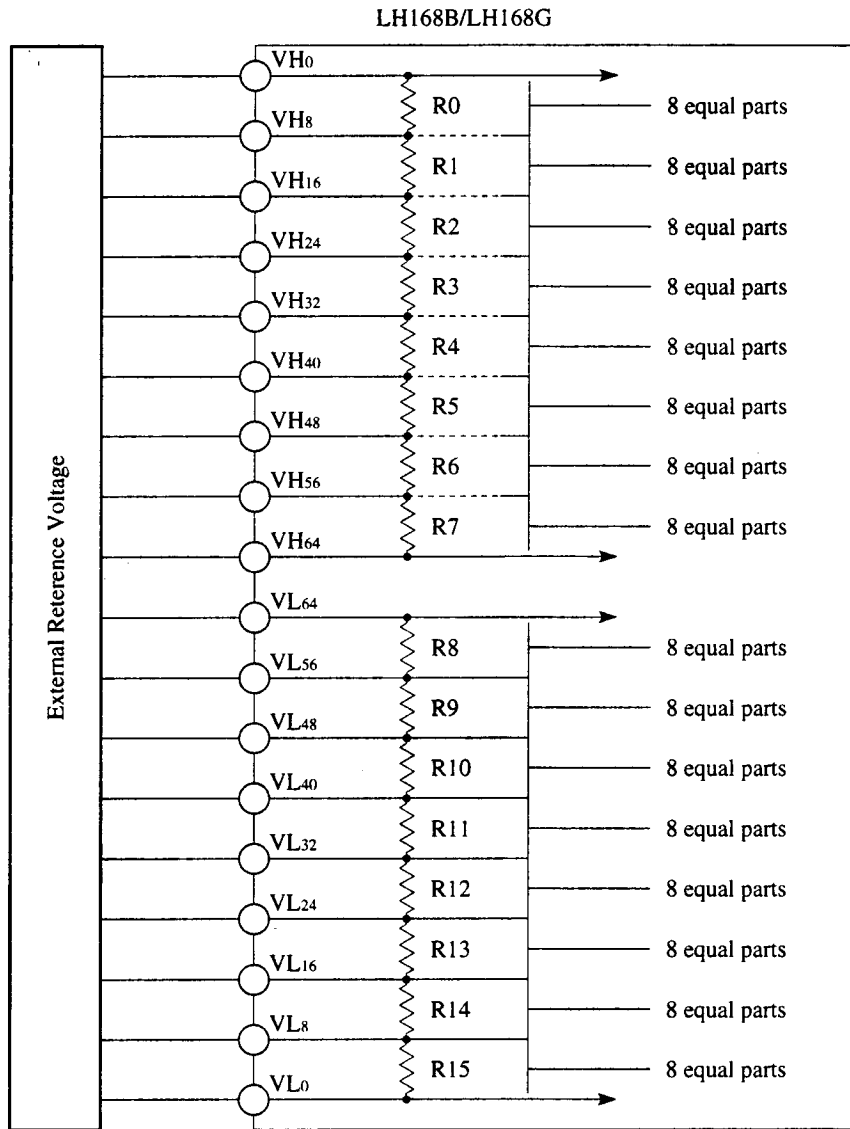
(4) Output voltage value

Of the 6-bit data (D₅, D₄, D₃, D₂, D₁ and D₀) taken in by time sharing, two reference voltages of reference voltage input V₀ to V₆₄ are selected by upper 3 bits (D₅, D₄ and D₃) and interpolation value divided two reference voltage into equal parts are determined by lower 3 bits (D₂, D₁, and D₀). The basic voltage V_i is reference voltage (V_H_i or V_L_i) that determined by polarity exchange input (REV, REV₂). Relation between input data and output voltage values is shown below.

Input data	Output voltage		Input data	Output voltage	
	POLA (POLB) = "Low"	POLA (POLB) = "High"		POLA (POLB) = "Low"	POLA (POLB) = "High"
0	V ₀	V ₆₄ + (V ₅₆ - V ₆₄) × 1/8	20	V ₃₂	V ₃₂ + (V ₂₄ - V ₃₂) × 1/8
1	V ₈ + (V ₀ - V ₈) × 7/8	V ₆₄ + (V ₅₆ - V ₆₄) × 2/8	21	V ₄₀ + (V ₃₂ - V ₄₀) × 7/8	V ₃₂ + (V ₂₄ - V ₃₂) × 2/8
2	V ₈ + (V ₀ - V ₈) × 6/8	V ₆₄ + (V ₅₆ - V ₆₄) × 3/8	22	V ₄₀ + (V ₃₂ - V ₄₀) × 6/8	V ₃₂ + (V ₂₄ - V ₃₂) × 3/8
3	V ₈ + (V ₀ - V ₈) × 5/8	V ₆₄ + (V ₅₆ - V ₆₄) × 4/8	23	V ₄₀ + (V ₃₂ - V ₄₀) × 5/8	V ₃₂ + (V ₂₄ - V ₃₂) × 4/8
4	V ₈ + (V ₀ - V ₈) × 4/8	V ₆₄ + (V ₅₆ - V ₆₄) × 5/8	24	V ₄₀ + (V ₃₂ - V ₄₀) × 4/8	V ₃₂ + (V ₂₄ - V ₃₂) × 5/8
5	V ₈ + (V ₀ - V ₈) × 3/8	V ₆₄ + (V ₅₆ - V ₆₄) × 6/8	25	V ₄₀ + (V ₃₂ - V ₄₀) × 3/8	V ₃₂ + (V ₂₄ - V ₃₂) × 6/8
6	V ₈ + (V ₀ - V ₈) × 2/8	V ₆₄ + (V ₅₆ - V ₆₄) × 7/8	26	V ₄₀ + (V ₃₂ - V ₄₀) × 2/8	V ₃₂ + (V ₂₄ - V ₃₂) × 7/8
7	V ₈ + (V ₀ - V ₈) × 1/8	V ₅₆	27	V ₄₀ + (V ₃₂ - V ₄₀) × 1/8	V ₂₄
8	V ₈	V ₅₆ + (V ₄₈ - V ₅₆) × 1/8	28	V ₄₀	V ₂₄ + (V ₁₆ - V ₂₄) × 1/8
9	V ₁₆ + (V ₈ - V ₁₆) × 7/8	V ₅₆ + (V ₄₈ - V ₅₆) × 2/8	29	V ₄₈ + (V ₄₀ - V ₄₈) × 7/8	V ₂₄ + (V ₁₆ - V ₂₄) × 2/8
A	V ₁₆ + (V ₈ - V ₁₆) × 6/8	V ₅₆ + (V ₄₈ - V ₅₆) × 3/8	2A	V ₄₈ + (V ₄₀ - V ₄₈) × 6/8	V ₂₄ + (V ₁₆ - V ₂₄) × 3/8
B	V ₁₆ + (V ₈ - V ₁₆) × 5/8	V ₅₆ + (V ₄₈ - V ₅₆) × 4/8	2B	V ₄₈ + (V ₄₀ - V ₄₈) × 5/8	V ₂₄ + (V ₁₆ - V ₂₄) × 4/8
C	V ₁₆ + (V ₈ - V ₁₆) × 4/8	V ₅₆ + (V ₄₈ - V ₅₆) × 5/8	2C	V ₄₈ + (V ₄₀ - V ₄₈) × 4/8	V ₂₄ + (V ₁₆ - V ₂₄) × 5/8
D	V ₁₆ + (V ₈ - V ₁₆) × 3/8	V ₅₆ + (V ₄₈ - V ₅₆) × 6/8	2D	V ₄₈ + (V ₄₀ - V ₄₈) × 3/8	V ₂₄ + (V ₁₆ - V ₂₄) × 6/8
E	V ₁₆ + (V ₈ - V ₁₆) × 2/8	V ₅₆ + (V ₄₈ - V ₅₆) × 7/8	2E	V ₄₈ + (V ₄₀ - V ₄₈) × 2/8	V ₂₄ + (V ₁₆ - V ₂₄) × 7/8
F	V ₁₆ + (V ₈ - V ₁₆) × 1/8	V ₄₈	2F	V ₄₈ + (V ₄₀ - V ₄₈) × 1/8	V ₁₆
10	V ₁₆	V ₄₈ + (V ₄₀ - V ₄₈) × 1/8	30	V ₄₈	V ₁₆ + (V ₈ - V ₁₆) × 1/8
11	V ₂₄ + (V ₁₆ - V ₂₄) × 7/8	V ₄₈ + (V ₄₀ - V ₄₈) × 2/8	31	V ₅₆ + (V ₄₈ - V ₅₆) × 7/8	V ₁₆ + (V ₈ - V ₁₆) × 2/8
12	V ₂₄ + (V ₁₆ - V ₂₄) × 6/8	V ₄₈ + (V ₄₀ - V ₄₈) × 3/8	32	V ₅₆ + (V ₄₈ - V ₅₆) × 6/8	V ₁₆ + (V ₈ - V ₁₆) × 3/8
13	V ₂₄ + (V ₁₆ - V ₂₄) × 5/8	V ₄₈ + (V ₄₀ - V ₄₈) × 4/8	33	V ₅₆ + (V ₄₈ - V ₅₆) × 5/8	V ₁₆ + (V ₈ - V ₁₆) × 4/8
14	V ₂₄ + (V ₁₆ - V ₂₄) × 4/8	V ₄₈ + (V ₄₀ - V ₄₈) × 5/8	34	V ₅₆ + (V ₄₈ - V ₅₆) × 4/8	V ₁₆ + (V ₈ - V ₁₆) × 5/8
15	V ₂₄ + (V ₁₆ - V ₂₄) × 3/8	V ₄₈ + (V ₄₀ - V ₄₈) × 6/8	35	V ₅₆ + (V ₄₈ - V ₅₆) × 3/8	V ₁₆ + (V ₈ - V ₁₆) × 6/8
16	V ₂₄ + (V ₁₆ - V ₂₄) × 2/8	V ₄₈ + (V ₄₀ - V ₄₈) × 7/8	36	V ₅₆ + (V ₄₈ - V ₅₆) × 2/8	V ₁₆ + (V ₈ - V ₁₆) × 7/8
17	V ₂₄ + (V ₁₆ - V ₂₄) × 1/8	V ₄₀	37	V ₅₆ + (V ₄₈ - V ₅₆) × 1/8	V ₈
18	V ₂₄	V ₄₀ + (V ₃₂ - V ₄₀) × 1/8	38	V ₅₆	V ₈ + (V ₀ - V ₈) × 1/8
19	V ₃₂ + (V ₂₄ - V ₃₂) × 7/8	V ₄₀ + (V ₃₂ - V ₄₀) × 2/8	39	V ₆₄ + (V ₅₆ - V ₆₄) × 7/8	V ₈ + (V ₀ - V ₈) × 2/8
1A	V ₃₂ + (V ₂₄ - V ₃₂) × 6/8	V ₄₀ + (V ₃₂ - V ₄₀) × 3/8	3A	V ₆₄ + (V ₅₆ - V ₆₄) × 6/8	V ₈ + (V ₀ - V ₈) × 3/8
1B	V ₃₂ + (V ₂₄ - V ₃₂) × 5/8	V ₄₀ + (V ₃₂ - V ₄₀) × 4/8	3B	V ₆₄ + (V ₅₆ - V ₆₄) × 5/8	V ₈ + (V ₀ - V ₈) × 4/8
1C	V ₃₂ + (V ₂₄ - V ₃₂) × 4/8	V ₄₀ + (V ₃₂ - V ₄₀) × 5/8	3C	V ₆₄ + (V ₅₆ - V ₆₄) × 4/8	V ₈ + (V ₀ - V ₈) × 5/8
1D	V ₃₂ + (V ₂₄ - V ₃₂) × 3/8	V ₄₀ + (V ₃₂ - V ₄₀) × 6/8	3D	V ₆₄ + (V ₅₆ - V ₆₄) × 3/8	V ₈ + (V ₀ - V ₈) × 6/8
1E	V ₃₂ + (V ₂₄ - V ₃₂) × 2/8	V ₄₀ + (V ₃₂ - V ₄₀) × 7/8	3E	V ₆₄ + (V ₅₆ - V ₆₄) × 2/8	V ₈ + (V ₀ - V ₈) × 7/8
1F	V ₃₂ + (V ₂₄ - V ₃₂) × 1/8	V ₃₂	3F	V ₆₄ + (V ₅₆ - V ₆₄) × 1/8	V ₀

(5) γ (gamma) correction value

Between reference voltage input pin VH_0 and VH_{64} , 64 resistors are connected in series. And between reference voltage input pin VL_0 and VL_{64} , 64 resistors are connected in series. And between reference voltage input pin VH_{64} and VL_{64} , a resistor isn't connected. The γ correction curve is broken line connected between intermediate voltage input ($VH_8, VH_{16}, VH_{24}, VH_{32}, VH_{40}, VH_{48}, VH_{56}, VL_8, VL_{16}, VL_{24}, VL_{32}, VL_{40}, VL_{48}$ and VL_{56}). Between the intermediate voltage input, it is divided into 8 parts by the same resistor.



The following shows the ratio of γ correction resistance, when R_0 equals 1.

R0	1.00
R1	0.50
R2	0.50
R3	0.50
R4	0.50
R5	0.50
R6	0.50
R7	1.00

R8	1.00
R9	0.50
R10	0.50
R11	0.50
R12	0.50
R13	0.50
R14	0.50
R15	1.00

■ Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC}	T _a = 25 °C	-0.3 to +7.0	V
	V _{LS}	T _a = 25 °C	-0.3 to +15.0	V
Input voltage	V _{H0} -V _{L0}	T _a = 25 °C	-0.3 to V _{LS} + 0.3	V
	Other	T _a = 25 °C	-0.3 to V _{CC} + 0.3	V
Output voltage	SPIO, SPOI	T _a = 25 °C	-0.3 to V _{CC} + 0.3	V
	XO ₁ -ZO ₁₀₈	T _a = 25 °C	-0.3 to V _{LS} + 0.3	V
Storage temperature	T _{stg}		-45 to +125	°C

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V _{CC}	2.7		3.6	V	
	V _{LS}	8.0		13.0	V	
Reference voltage input	V _{H0} -V _{H64}	0.5V _{LS}		V _{LS} - 0.1	V	1
	V _{L0} -V _{L64}	+0.1		0.5V _{LS}	V	
Clock frequency	f _{ck}			55	MHz	
LCD drive output load capacity	C _L			150	pF	
Operating temperature	T _{opr}	-20		75	°C	

Note 1. Observe the following relation for the potential of the reference voltage input.

V_{LS} > V_{H0} > V_{H8} > V_{H16} > V_{H24} > V_{H32} > V_{H40} > V_{H48} > V_{H56} > V_{H64} ≥ 0.5V_{LS} ≥ V_{L64} > V_{L56} > V_{L48} > V_{L40} > V_{L32} > V_{L24} > V_{L16} > V_{L8} > V_{L0} > GND

Note 2. Observe the following sequence of switching power supply on the device.

V_{CC} → Logic input → V_{LS}, V_{H0}-V_{H64}, V_{L64}-V_{L0}

Observe the contrary sequence of switching power supply off the device.

■ DC Electrical Characteristics

(V_{CC} = 2.7 to 3.6 V, V_{LS} = 8.0 to 13 V, T_a = -20 to +75 °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Input "Low" current	I _{IL}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, REV ₂ , POLA, POLB, MODE, PBS			10	μA
Input "High" current	I _{ILH1}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, MODE, PBS			10	μA
	I _{ILH2}		POLA, POLB, REV ₂			400	μA
Input "Low" voltage	V _{IL}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, REV ₂ , POLA, POLB, MODE, PBS	GND		0.3V _{CC}	V
Input "High" voltage	V _{IH}		XA ₀ -XA ₅ , YA ₀ -YA ₅ , ZA ₀ -ZA ₅ , XB ₀ -XB ₅ , YB ₀ -YB ₅ , ZB ₀ -ZB ₅ , SPIO, SPOI, CK, LS, LBR, REV, REV ₂ , POLA, POLB, MODE, PBS	0.7V _{CC}		V _{CC}	V
Output "Low" voltage	V _{OL}	I _{OL} = 0.3 mA	SPIO	GND		GND + 0.4	V
Output "High" voltage	V _{OH}	I _{OH} = -0.3 mA	SPOI	V _{CC} - 0.4		V _{CC}	V
Current consumption (In operation mode)	I _{CC1}	*1	V _{CC} - GND			12	mA
Current consumption (Instandby mode)	I _{CC2}	*2	V _{CC} - GND			4.0	mA
Current consumption (In operation mode)	I _{LS1}	*1	V _{LS} - GND			8.0	mA
Current consumption (In standby mode)	I _{LS2}	*2	V _{LS} - GND			7.0	mA
Output voltage range	V _{OUT}			GND + 0.2		V _{LS} - 0.2	V
Deviations between output voltage pins	V _{OD}		XO ₁ - ZO ₁₀₈	-20		+20	mV
Output current	I _{O1} -I _{O4}	*3			200		μA
Resistance between reference power supplies	R _{GMAH}		Between VH ₀ and VH ₆₄		20		kΩ
	R _{GMAL}		Between VL ₀ and VL ₆₄		20		kΩ

[Measuring condition]

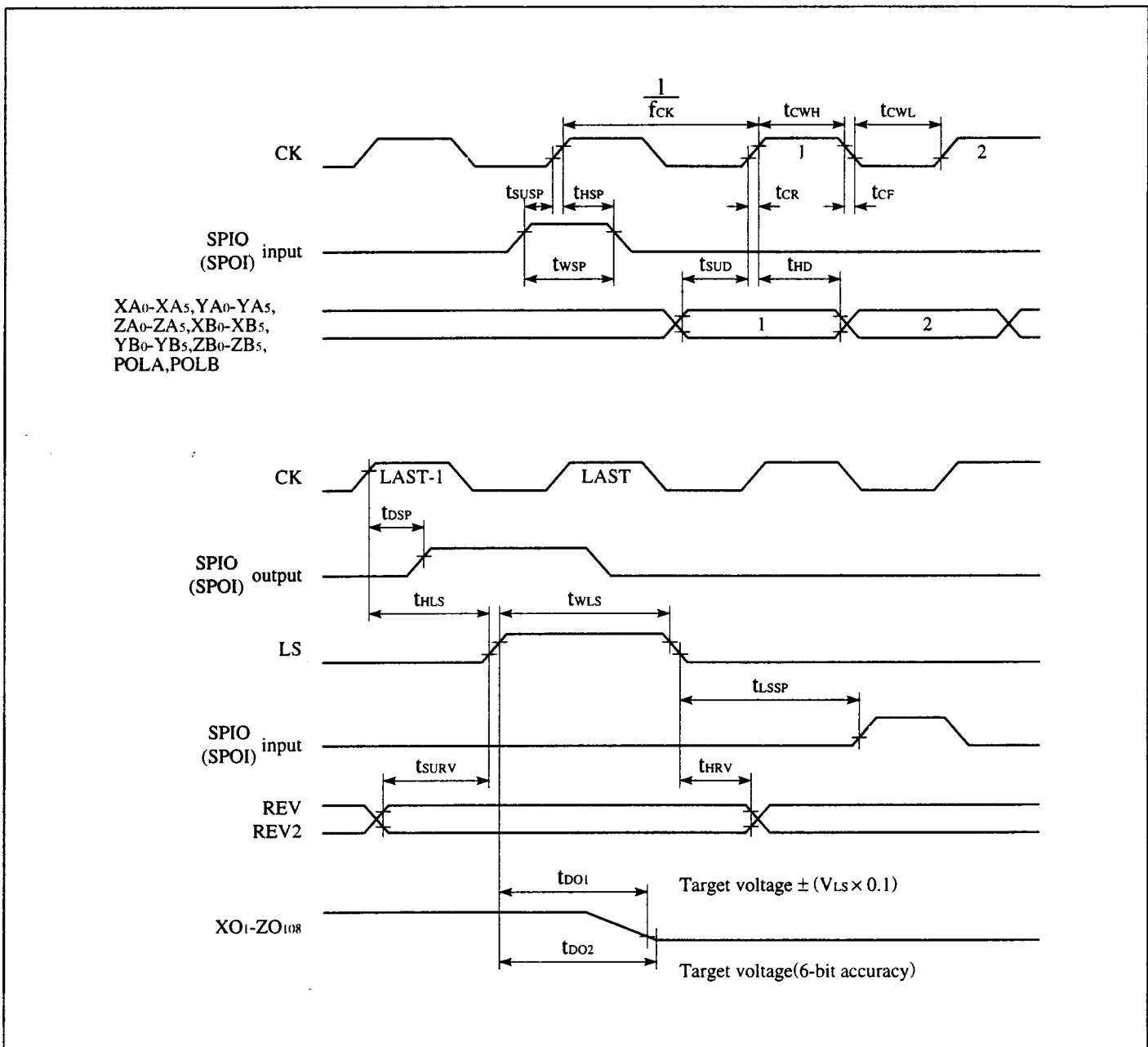
- *1 f_{CK} = 55 MHz, f_{LS} = 50 kHz (Data sampling state)
- *2 f_{CK} = 55 MHz, f_{LS} = 50 kHz, SPI = GND is fixed. (Standby state)
- *3
 - I_{O1}
 - Applied voltage = 8.0 V for output pins XO₁-ZO₁₀₈
 - Output voltage = 7.5 V for output pins XO₁-ZO₁₀₈
 - V_{LS} = 10V
 - I_{O2}
 - Applied voltage = 7.0 V for output pins XO₁-ZO₁₀₈
 - Output voltage = 7.5 V for output pins XO₁-ZO₁₀₈
 - V_{LS} = 10V
 - I_{O3}
 - Applied voltage = 3.0 V for output pins XO₁-ZO₁₀₈
 - Output voltage = 2.5 V for output pins XO₁-ZO₁₀₈
 - V_{LS} = 10V
 - I_{O4}
 - Applied voltage = 2.0 V for output pins XO₁-ZO₁₀₈
 - Output voltage = 2.5 V for output pins XO₁-ZO₁₀₈
 - V_{LS} = 10 V

■ AC Electrical Characteristics

(V_{CC} = 2.7 to 3.6 V, V_{LS} = 8.0 to 13 V, T_a = -20 to +75 °C)

Parameter	Symbol	Measuring condition	Applicable pin	MIN.	TYP.	MAX.	Unit
Clock frequency	f _{CK}		CK			55	MHz
"High" level pulse width	t _{CWH}			4.0			ns
"Low" level pulse width	t _{CWL}			4.0			ns
Input rise time	t _{CR}					10	ns
Input fall time	t _{CF}					10	ns
Data setup time	t _{SUD}		XA ₀ -XA ₅ , XB ₀ -XB ₅ , YA ₀ -YA ₅ , YB ₀ -YB ₅ , ZA ₀ -ZA ₅ , ZB ₀ -ZB ₅ , POLA, POLB	4.0			ns
Data hold time	t _{HD}			0			ns
Start pulse setup time	t _{SUSP}		SPIO, SPOI	4.0			ns
Start pulse hold time	t _{HSP}		SPIO, SPOI	0			ns
Start pulse width	t _{WSP}		SPIO, SPOI			$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t _{DSP}	C _L = 15 pF	SPIO, SPOI			12	ns
LCD drive output delay time	t _{DO1}	C _L = 150 pF	XO ₁ -XO ₁₀₈			3	μs
	t _{DO2}	C _L = 150 pF				10	μs
LS signal, SPI signal setup time	t _{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal, CK signal hold time	t _{HLS}		LS	7			ns
LS signal "High" level width	t _{WLS}		LS	$\frac{1}{f_{CK}}$			ns
REV signal, LS signal setup time	t _{SURV}		REV, REV ₂	14			ns
REV signal, LS signal hold time	t _{HRV}		REV, REV ₂	10			ns

■ Timing Diagram



■ Example of Typical Characteristics

($T_a = 25\text{ }^\circ\text{C}$, GND = 0 V, $V_{CC} = 3.3\text{ V}$)

Parameter	MIN.	TYP.	MAX.	Unit
Basic gate propagation delay time		10		ns

■ Sharp's Product Line-up (TFT LCD Driver)

★ Under development

Model No.	Display panel	Drive function	Gray scale	Output	Display (V) MAX.	Clock frequency (Hz) MAX.	Supply voltage (V)	Description	Package
LH1689F	for OA (VGA)	Source	64-scale (6-bit)	240	5.5	55M	3.0 to 5.5	Built-in reference voltage generation circuit, R-DAC system	SST
LH1685F	for OA (SVGA/XGA)	Source	64-scale (6-bit)	309/300	5.5	55M	3.0 to 5.5	Built-in reference voltage generation circuit, R-DAC system	SST
LH168BF LH168GF	for OA (XGA)	Source	64-scale (6-bit)	324/312	13	55M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
LH168DF LH168JF	for OA (XGA/SXGA)	Source	64-scale (6-bit)	384	13	65M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
★ LH168EF	for OA (XGA/SXGA)	Source	256-scale (8-bit)	384	13	65M	2.7 to 3.6	Dot inversion drive, Built-in reference voltage generation circuit	SST
★ LH168AF	for OA (SVGA/XGA)	Source	64-scale (6-bit)	384	5.5	55M	2.7 to 3.6	2-port data input, Built-in reference voltage generation circuit, R-DAC system	SST
LH1684F	for AV	Source	Analog	240	5.5	10M	4.5 to 5.5	Three-point simultaneous or sequential sampling selectable. Sampling frequency : 20 MHz	SST
★ LH1687F	for AV	Source	Analog	240	5.5	12.5M	3.0 to 5.5	Three-point simultaneous or sequential sampling selectable. Sampling frequency : 25 MHz. Power save function	SST
LH1691F	for OA/AV (VGA)	Gate	—	240	33	100k	3.0 to 5.5	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable. Both positive/negative power supply capability	SST
LH1692F	for OA (SVGA)	Gate	—	300	42	100k	3.0 to 5.5	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable. Both positive/negative power supply capability	SST
LH1694F	for OA (XGA/SXGA)	Gate	—	256	42	100k	2.7 to 3.6	1-pulse (normal) or 2-pulse (normal/precharge) scanning selectable. Both positive/negative power supply capability. Enable chain cascade connection	SST

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